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PATENT ABSTRACTS OF JAPAN

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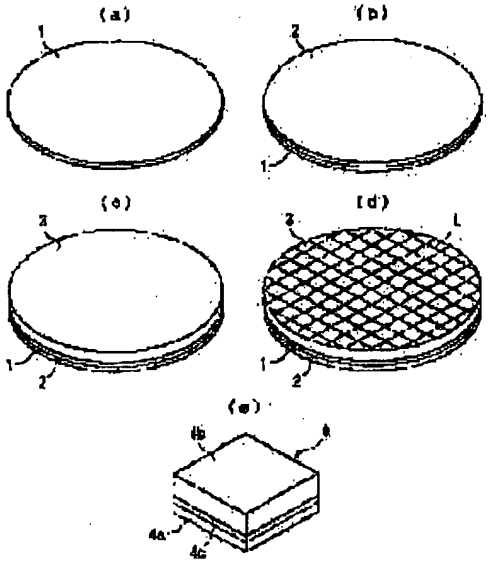
(54) MANUFACTURING METHD OF SEMICONDUCTOR BARE CHIP

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain semiconductor bare chips having radiation plates integrated therewith, by such a simple procedure that after sticking one radiation plate on a wafer, the resultant product is merely divided into the bare chips.

SOLUTION: On a wafer 1, electronic circuits are formed in a predetermined array. Then, to the rear surface of the wafer 1, a bonding material 2 is applied with a uniform thickness. As the bonding material 2, there is used a silicon bonding material having both an elasticity capable of absorbing a stressed strain caused by the difference between thermal expansion coefficients and an excellent thermal conductivity. Then, on the coated surface of the wafer 1 with the bonding material 2, a radiation plate 3 having the same outer diameter as the wafer 1 and made of a thermally conductive metal is so stuck that no bubble is included between them. Then, pressing relatively the radiation plate 3 against the wafer 1, the excess bonding material 2 is extruded from between the wafer 1 and the radiation plate 3 to make the thickness of the bonding material 2 as small as possible. Then, dividing the wafer 1 with the stuck radiation plate 3 thereon into individual chips by lines L laid along the boundaries among the formed circuits, semiconductor bare chips 4 are obtained.



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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the semi-conductor bare chip characterized by what the wafer with which the heat sink was stretched is divided into each chip for after an electronic circuitry makes a heat sink rival through a binder at the rear face of the wafer formed in the predetermined array.
[Claim 2] The manufacture approach of the semi-conductor bare chip according to claim 1 characterized by what a heat sink is forced relatively [wafer] before binder hardening, and an excessive binder is extruded for.
[Claim 3] The manufacture approach of the semi-conductor bare chip according to claim 1 or 2 characterized by the thing using the silicon system binder as a binder.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the semi-conductor bare chip connected to the circuit board etc. by the flip-chip-bonding method.
[0002]
[Description of the Prior Art] This kind of semi-conductor bare chip is manufactured by dividing this wafer into each chip with the dicing method or a scriber, after carrying out processes, such as diffusion, puncturing, wiring, electrode formation, protective coat formation, and electrical property inspection, in the state of a wafer.
[0003] As a cure against heat dissipation of this semi-conductor bare chip, after carrying a semi-conductor bare chip in the circuit board, generally the method which attaches a heat sink in this through heat dissipation grease etc. is adopted.
[0004]
[Problem(s) to be Solved by the Invention] In addition to spreading of adhesives and heat dissipation grease, it has the trouble which requires the loading activity of a heat sink separately, and has the fault which cannot deny the increment in cost concerning post-installation while it needs to prepare the heat sink from which magnitude and thickness differ for every class of semi-conductor bare chip, since the above-mentioned conventional cure against heat dissipation is a method which post-installs a heat sink in a semi-conductor bare chip according to an individual.
[0005] This invention was made in view of the above-mentioned situation, and the place made into the purpose is to offer the manufacture approach of the semi-conductor bare chip which made post-installation of a heat sink unnecessary.
[0006]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the manufacture approach of the semi-conductor bare chip concerning this invention is characterized [the / main] by what the wafer with which the heat sink was stretched is divided into each chip for, after an electronic circuitry makes a heat sink rival through a binder at the rear face of the wafer formed in the predetermined array.
[0007] According to the manufacture approach of the semi-conductor bare chip concerning this invention, after sticking a heat sink on a wafer, the semi-conductor

bare chip which equipped one with the radiator in the easy procedure of separating this can be obtained.

[0008]

[Embodiment of the Invention] Drawing 1 shows 1 operation gestalt of this invention, and, for a wafer and 2, as for a heat sink and L, a binder and 3 are [one in drawing / separation Rhine and 4] semi-conductor bare chips.

[0009] On the occasion of manufacture of a semi-conductor bare chip, first, as shown in drawing 1 (a), processes, such as diffusion, puncturing, wiring, electrode formation, protective coat formation, and electrical property inspection, are carried out to the wafer 1 which consists of silicon, GaAs, etc., and electronic circuitries, such as IC and LSI, are formed in it in a predetermined array. Since the circuit formation procedure to a wafer 1 is the same as a well-known thing, explanation here is omitted.

[0010] Next, as shown in this drawing (b), a binder 2 is applied to the rear face (a circuit forming face is a field of the opposite side) of a wafer 1 by uniform thickness. Although it is possible to use various well-known binders for this binder 2, since there is a possibility that a wafer 1 and a heat sink 3 may be combined firmly, and a crack may occur by considering the stress-strain diagram by the difference of both coefficient of thermal expansion as a cause when solder, wax material, etc. are used, the silicon system binder which was excellent in thermal conductivity preferably with the resiliency which can absorb this stress-strain diagram is used.

[0011] Next, as shown in this drawing (c), as air bubbles do not go into the binder spreading side of a wafer 1, they stick on it the heat sink 3 which consists of metals, such as the heat sink which has the same outer diameter as a wafer 1, for example, thermally conductive good gold, silver, and aluminum. Of course, after applying the above-mentioned binder 2 to the whole surface of a heat sink 3, you may make it make this rival the circuit forming face of a wafer 1 in the field of the opposite side. The thickness of a heat sink 3 is suitably selected according to the calorific value of the electronic circuitry formed in the wafer 1.

[0012] And a heat sink 3 is forced relatively [wafer / 1] before binder hardening, the excessive binder 2 is extruded from between a wafer 1 and heat sinks 3, and the thickness is made thin as much as possible. The extruded binder is removed after hardening.

[0013] Next, as shown in this drawing (d), the wafer 1 with which the heat sink 3 was stretched is divided into the chip of each [Rhine L which met the boundary of a formation circuit with the well-known dicing method and a well-known scriber], and the semi-conductor bare chip 4 as shown in this drawing (e) is obtained.

[0014] This semi-conductor bare chip 4 has the structure which rectangle-like chip section 4a and radiator 4b combined up and down through binder layer 4c, and as radiator 4b turns to it outside, it is connected to the circuit board etc. by the flip-chip-bonding method.

[0015] Since according to the above-mentioned operation gestalt the semi-conductor bare chip 4 which equipped one with radiator 4b in the easy procedure of separating this can be obtained after sticking a heat sink 3 on a wafer 1, there is no trouble which post-installs a heat sink according to an individual in a semi-

conductor bare chip like before, and there is an advantage which can avoid the increment in cost concerning post-installation.

[0016] Moreover, if the silicon system binder which was excellent in thermal conductivity with resiliency as a binder 2 is used, there is an advantage which absorbs the stress-strain diagram by the difference of the coefficient of thermal expansion of a wafer 1 and a heat sink 3, and can prevent crack initiation beforehand.

[0017]

[Effect of the Invention] As explained in full detail above, since according to this invention the semi-conductor bare chip which equipped one with the radiator in the easy procedure of separating this can be obtained after sticking a heat sink on a wafer, there is no trouble which post-installs a heat sink according to an individual in a semi-conductor bare chip like before, and there is an advantage which can avoid the increment in cost concerning post-installation.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing 1 operation gestalt of this invention
[Description of Notations]
1 [— Separation Rhine, 4 / — A semi-conductor bare chip, 4a / — The chip section, 4b / — A radiator, 4c / — Binder layer.] — A wafer, 2 — A binder, 3 — A heat sink, L

[Translation done.]

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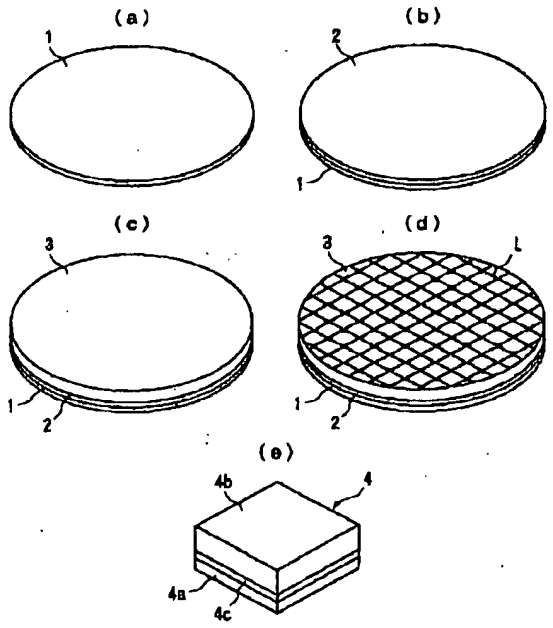
最終頁に続く

(54)【発明の名称】 半導体ベアチップの製造方法

(57)【要約】
【課題】 放熱板の後付けを不要とした半導体ベアチップの製造方法を提供する。
【解決手段】 電子回路が所定配列で形成されたウエファ１の裏面に接着材２を介して放熱板３を張り合わせた後、放熱板３が張り合わされたウエファ１を個々のチップに分離することにより、放熱部４ｂを一体に備えた半導体ベアチップ４を得る。



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【特許請求の範囲】

【請求項１】 電子回路が所定配列で形成されたウエファの裏面に接着材を介して放熱板を張り合わせた後、放熱板が張り合わされたウエファを個々のチップに分離する、

ことを特徴とする半導体ベアチップの製造方法。

【請求項２】 接着材硬化前に放熱板をウエファに相対的に押し付けて余分な接着材を押し出す、

ことを特徴とする請求項１記載の半導体ベアチップの製造方法。

【請求項３】 接着材としてシリコン系接着材を用いた、

ことを特徴とする請求項１または２記載の半導体ベアチップの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、フリップチップボンディング法によって回路基板等に接続される半導体ベアチップの製造方法に関するものである。

【０００２】

【従来の技術】この種の半導体ベアチップは、ウエファの状態で拡散，開孔，配線，電極形成，保護膜形成，電気特性検査等の工程を実施した後、該ウエファをダイシング法やスクライバ法によって個々のチップに分離することにより製造されている。

【０００３】この半導体ベアチップの放熱対策としては、半導体ベアチップを回路基板に搭載した後これに放熱グリス等を介して放熱板を取り付ける方式が一般に採用されている。

【０００４】

【発明が解決しようとする課題】上記従来の放熱対策は、半導体ベアチップに個別に放熱板を後付けする方式であるため、半導体ベアチップの種類毎に大きさや厚みの異なる放熱板を用意する必要があると共に、接着剤や放熱グリスの塗布作業に加え、放熱板の搭載作業を別途要する面倒があり、後付けに係るコスト増加を否めない不具合がある。

【０００５】本発明は上記事情に鑑みてなされたもので、その目的とするところは、放熱板の後付けを不要とした半導体ベアチップの製造方法を提供することにある。

【０００６】

【課題を解決するための手段】上記目的を達成するため、本発明に係る半導体ベアチップの製造方法は、電子回路が所定配列で形成されたウエファの裏面に接着材を介して放熱板を張り合わせた後、放熱板が張り合わされたウエファを個々のチップに分離する、ことをその主たる特徴としている。

【０００７】本発明に係る半導体ベアチップの製造方法によれば、ウエファに放熱板を張り付けてからこれを分離するだけの簡単な手順にて、放熱部を一体に備えた半導体ベアチップを得ることができる。

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【０００８】

【発明の実施の形態】図１は本発明の一実施形態を示すもので、図中の１はウエファ、２は接着材、３は放熱板、Ｌは分離ライン、４は半導体ベアチップである。

【０００９】半導体ベアチップの製造に際しては、まず、図１（ａ）に示すように、シリコン，ＧａＡｓ等から成るウエファ１に、拡散，開孔，配線，電極形成，保護膜形成，電気特性検査等の工程を実施してＩＣ，ＬＳＩ等の電子回路を所定配列で形成する。ウエファ１への回路形成手順は周知のものと同じであるためここでの説明を省略する。

【００１０】次に、同図（ｂ）に示すように、ウエファ１の裏面（回路形成面とは反対側の面）に接着材２を均一な厚みで塗布する。この接着材２には周知の接着材を種々用いることが可能であるが、半田やろう材等を用いるとウエファ１と放熱板３とが強固に結合され、両者の熱膨張係数の差による応力歪みを原因としてクラックが発生する恐れがあるので、好ましくは、この応力歪みを吸収可能な弾力性を持ち且つ熱伝導性に優れたシリコン系接着材を使用する。

【００１１】次に、同図（ｃ）に示すように、ウエファ１の接着材塗布面に、ウエファ１と同一外径を有する放熱板、例えば熱伝導性の良い金，銀，アルミニウム等の金属から成る放熱板３を気泡が入らぬようにして張り付ける。勿論、放熱板３の一面に上記接着材２を塗布してから、これをウエファ１の回路形成面とは反対側の面に張り合わせるようにしてもよい。放熱板３の厚みはウェファ１に形成された電子回路の発熱量に応じて適宜選定される。

【００１２】そして、接着材硬化前に放熱板３をウエファ１に相対的に押し付け、ウエファ１と放熱板３の間から余分な接着材２を押し出してその厚みを極力薄くする。押し出された接着材は硬化後に取り除く。

【００１３】次に、同図（ｄ）に示すように、放熱板３が張り合わされたウエファ１を、周知のダイシング法やスクライバ法によって形成回路の境界に沿ったラインＬで個々のチップに分離し、同図（ｅ）に示すような半導体ベアチップ４を得る。

【００１４】この半導体ベアチップ４は、矩形状のチップ部４ａと放熱部４ｂとが接着材層４ｃを介して上下に結合した構造を有しており、放熱部４ｂが外側に向くようにしてフリップチップボンディング法により回路基板等に接続される。

【００１５】上述の実施形態によれば、ウエファ１に放熱板３を張り付けてからこれを分離するだけの簡単な手順にて、放熱部４ｂを一体に備えた半導体ベアチップ４を得ることができるので、従来のように半導体ベアチップに個別に放熱板を後付けする面倒がなく、後付けに係

るコスト増加を回避できる利点がある。

【００１６】また、接着材２として、弾力性を持ち且つ熱伝導性に優れたシリコン系接着材を用いれば、ウエファ１と放熱板３との熱膨張係数の差による応力歪みを吸収してクラック発生を未然に防止できる利点がある。

【００１７】

【発明の効果】以上詳述したように、本発明によれば、ウエファに放熱板を張り付けてからこれを分離するだけの簡単な手順にて、放熱部を一体に備えた半導体ベアチ＊

＊ップを得ることができるので、従来のように半導体ベアチップに個別に放熱板を後付けする面倒がなく、後付けに係るコスト増加を回避できる利点がある。

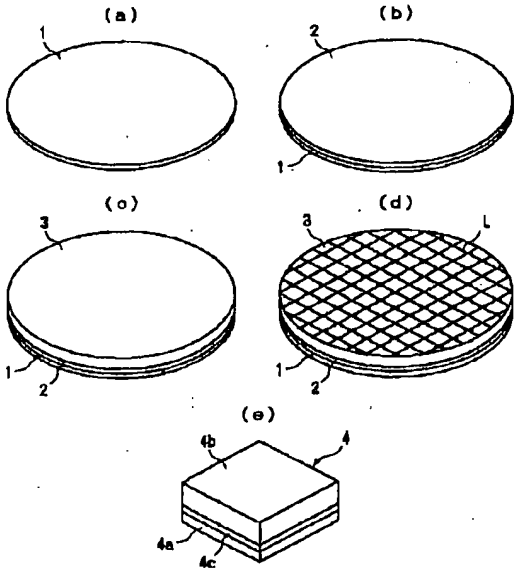
【図面の簡単な説明】

【図１】本発明の一実施形態を示す図

【符号の説明】

１…ウエファ、２…接着材、３…放熱板、Ｌ…分離ライン、４…半導体ベアチップ、４ａ…チップ部、４ｂ…放熱部、４ｃ…接着材層。

【図１】



フロントページの続き

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